REMARKS

The Office Action of 11/22/2006 has been carefully considered. Reconsideration and allowance in view of the present remarks is respectfully requested.

Claims 4-10 were indicated as containing allowable subject matter, which indication is appreciatively acknowledged.

Claims 1-3, 11 and 12 were rejected as being anticipated by de Jong. This rejection is respectfully traversed, and reconsideration is respectfully requested.

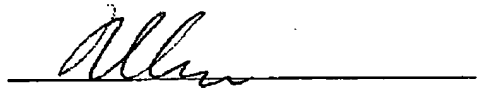
The rejection states in part "[d]e Jong et al. disclose...a test controller [comprising] a first register...for receiving a bit pattern via the input pin and outputting the bit pattern via the output pin...; a second register...for capturing the bit pattern responsive to an update signal...; and...dedicated control circuitry for blocking the update signal responsive to the bit pattern *(page 477-478, Dedicated Fast Flash Controller section; figure 8)*."

Applicant has diligently studied de Jong and does not find any such teaching of dedicated control circuitry for blocking the update signal responsive to the bit pattern. Such circuitry can be seen in Figure 1 of the present specification as elements 180 and 182, for example.

In de Jong, assuming the respective registers clocked by the clockDR and updateDR signals to correspond to the first and second registers as claimed, there is no evident structure in Figure 8 or Figure 9 of de Jong to perform the function of blocking the update signal responsive to the bit pattern, as claimed.

Withdrawal of the rejections and allowance of claims 1-18 is respectfully requested.

Respectfully submitted,



Michael J. Ure, Reg. 33,089

Dated: 02/21/2007